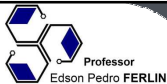
Professor  
Edson Pedro FERLIN

# Lógica Digital

*Prof. Edson Pedro Ferlin*

Professor  
Edson Pedro FERLIN

- **Objetivos**
  - Estudar os circuitos digitais presentes nos computadores
- **Conteúdos**
  - Funções Lógicas
  - Portas Lógicas
  - Circuitos Integrados
  - Álgebra de Boole (Booleana)
  - Circuitos Digitais
  - Circuitos Básicos

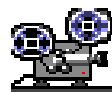
## Sistema Digital

É uma combinação de dispositivos projetados para manipular informação lógica ou quantidades físicas que são representadas no formato digital, ou seja, as quantidades podem assumir apenas valores discretos.

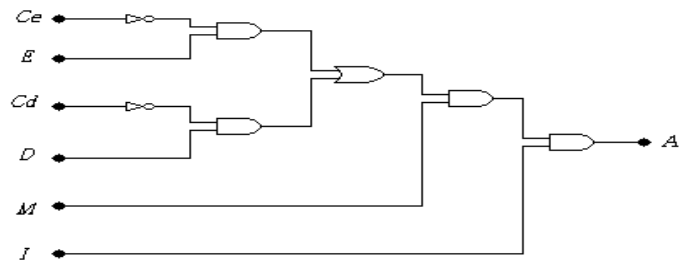
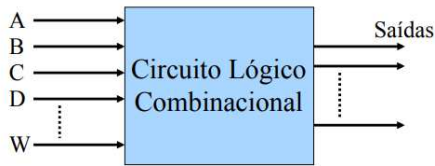
Tocci & Widmer  
Sistemas Digitais

## Portas Lógicas

Assista o vídeo sobre Portas Lógicas  
(link: <https://youtu.be/ckOBTc1XJik>).



## Circuito Combinacional



## Portas Lógicas

### Inversora



A	$X = A'$
0	1
1	0

### AND



A	B	$X = (A \cdot B)$
0	0	0
0	1	0
1	0	0
1	1	1

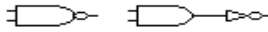
### OR



A	B	$X = (A \oplus B)$
0	0	0
0	1	1
1	0	1
1	1	0

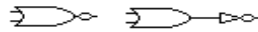
## Portas Lógicas (cont.)

### NAND



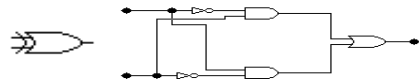
A	B	$X = (A \cdot B)'$
0	0	1
0	1	1
1	0	1
1	1	0

### NOR



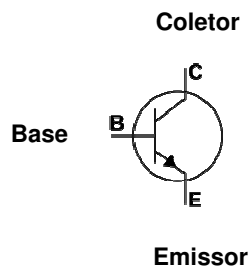
A	B	$X = (A + B)'$
0	0	1
0	1	0
1	0	0
1	1	0

### XOR



A	B	$X = (A \oplus B)$
0	0	0
0	1	1
1	0	1
1	1	0

## Transistor (Transference Resistor)



Base = 1 → circuito fechado

Base = 0 → circuito aberto

## Transistor (em corte)

**TRANSISTOR DE EFEITO DE CAMPO**

UM COMPONENTE FUNDAMENTAL para a construção de um microprocessador é o transistor de efeito de campo, que atua como um simples interruptor. A voltagem adequada aplicada ao eletrodo-porta induz uma carga ao longo do canal, que então conduz a corrente da fonte ao dreno, colocando o interruptor na posição ligada. Com portas suficientemente pequenas, esses transistores podem ser ligados e desligados bilhões de vezes por segundo.



TRANSISTOR de escala nanométrica de primeira geração, produzido pela Intel



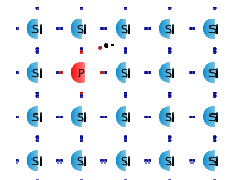
## Semicondutores

### Semicondutor

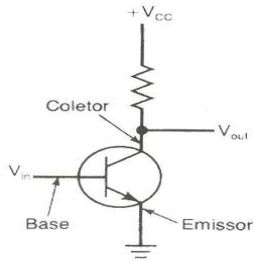
Si  
Ge  
GaAs

### Dopagem

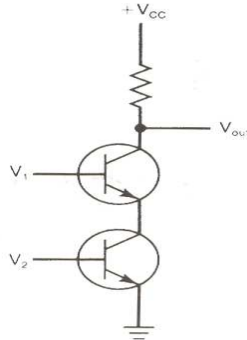
Tipo N  
Tipo P



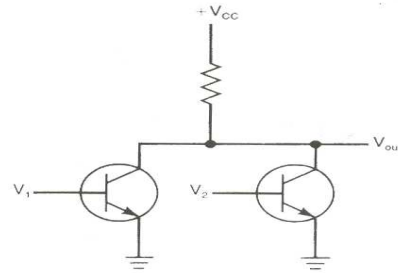
## Circuito Elétrico das Portas Lógicas



**Inversora**



**NAND**

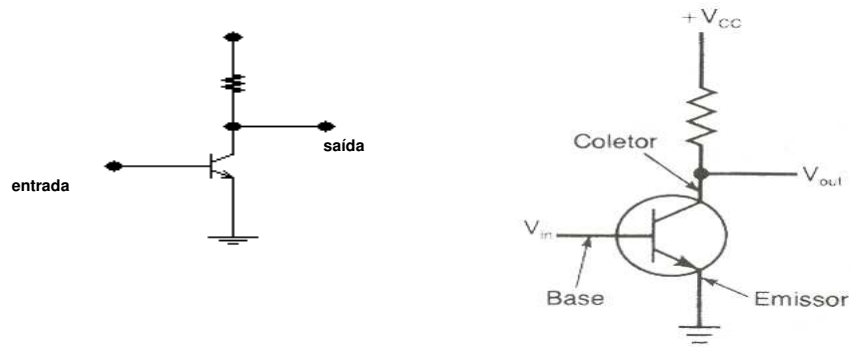


**NOR**

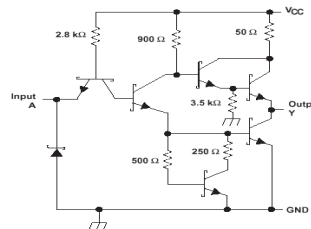
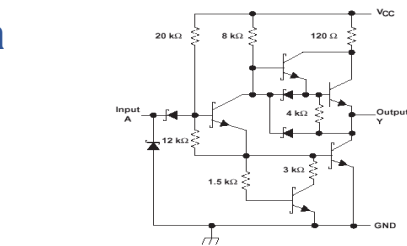
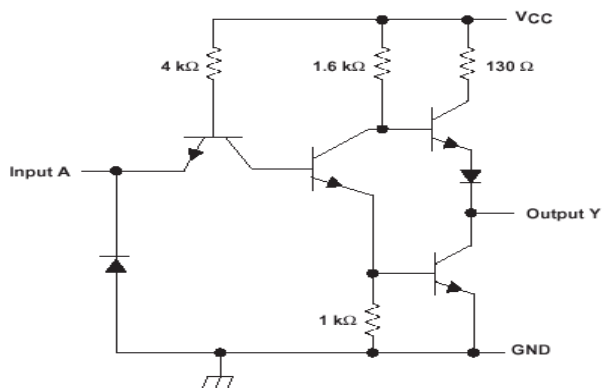
## Níveis Lógicos



## Porta Inversora



## Porta Inversora (7404)

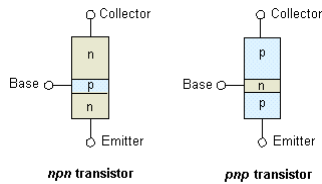


## Tecnologia de Famílias Lógicas

- **Bipolar** → TTL (*Transistor-Transistor Logic*)
- **MOS** → CMOS (*Complementary Metal-Oxide Semiconductor*)

## Tipos de Transistores

### Bipolar

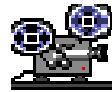


### MOSFET



## Circuitos Integrados

Assista o vídeo sobre Circuitos Integrados  
(link: <https://youtu.be/ti9VVBHljWU>).



**SN5486, SN54LS86A, SN54S86  
SN7486, SN74LS86A, SN74S86  
QUADUPLE 2-INPUT EXCLUSIVE-OR GATES**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	3 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S86	-55°C to 125°C
SN74S86	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network-ground terminal.

recommended operating conditions

	SN54S86			SN74S86			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-1			-1	mA
Low-level output current, $I_{OL}$			20			20	mA
Operating free-air temperature, $T_A$	-55	125	0	70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>1</sup>	SN54S86			SN74S86			UNIT
		MIN	TYP <sup>2</sup>	MAX	MIN	TYP <sup>2</sup>	MAX	
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}$ , $I_O = -18 \text{ mA}$	2		2			V	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $I_O = 20 \text{ mA}$	0.8		0.8			V	
$V_{IC}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$	-1.2		-1.2			V	
$V_{OH}$ High-level output voltage	$V_{CC} = 0.8 \text{ V}$ , $I_{OH} = -1 \text{ mA}$	2.5	3.4	2.7	3.4		V	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ $V_{OL} = 0.8 \text{ V}$ , $I_{OL} = 20 \text{ mA}$	0.5		0.5			V	
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$		1		1		mA	
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$		50		50		µA	
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.5 \text{ V}$		-2		-2		mA	
$I_{OHS}$ Short-circuit output current <sup>1</sup>	$V_{CC} = \text{MAX}$	-40	-100	-40	-100		mA	
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}$ , See Note 3		50		75		mA	

<sup>1</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable term. <sup>2</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ . <sup>3</sup>Flux more than one output should be avoided at a time, and duration at the short circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with the inputs grounded and the outputs open.

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

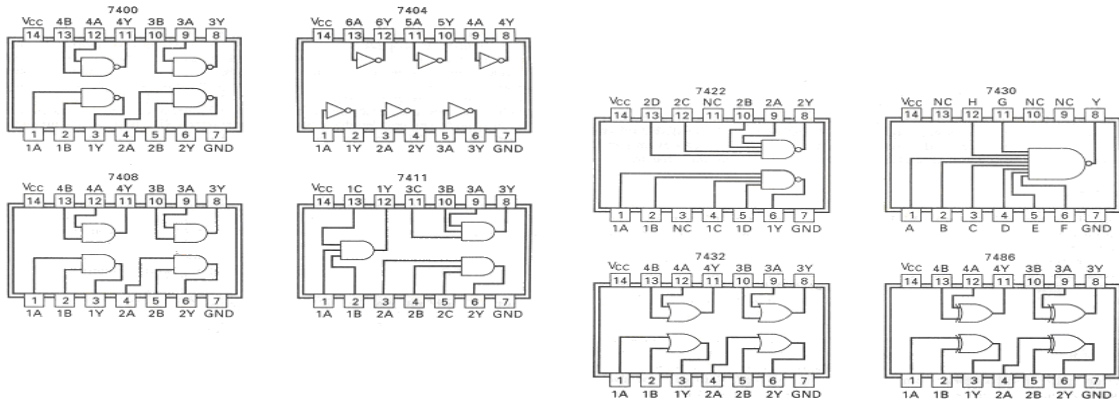
PARAMETER <sup>1</sup>	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	A or B	Other input low $C_L = 15 \text{ pF}$		7	10.5	ns
$t_{PHL}$	A or B	Other input high $R_L = 280 \Omega$		6.5	10	ns

<sup>1</sup> $t_{PLH}$  = propagation delay time, low-to-high-level output  
<sup>2</sup> $t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



## Circuito Integrado (*Layout*)



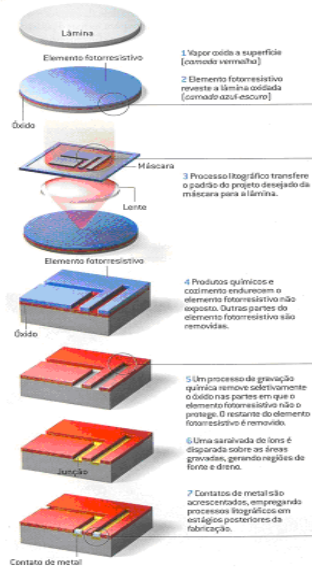
## Circuitos Integrados (CI)

- SSI (*Small Scale Integration*): até 10 portas
- MSI (*Medium Scale Integration*): 10 a 100 portas
- LSI (*Large Scale Integration*): 100 a 100.000 portas
- VLSI (*Very Large Scale Integration*): > 100.000 portas

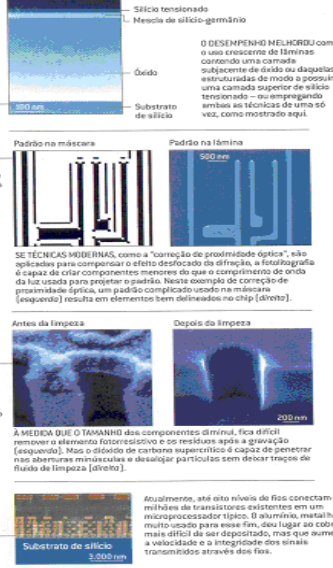
### O VELHO E O NOVO NA FABRICAÇÃO DE SEMICONDUTORES

UMA LÂMINA CIRCULAR de silício, do tamanho aproximado de um prato comum, é o ponto de partida para o processo de fabricação de chips em etapas, que esculpe em transistores e suas interconexões. Algumas das manipulações apresentadas abaixo são repetidas diversas vezes durante a produção para construir estruturas complexas, camada por camada.

#### PROCESSO BÁSICO DE FABRICAÇÃO DE CHIPS

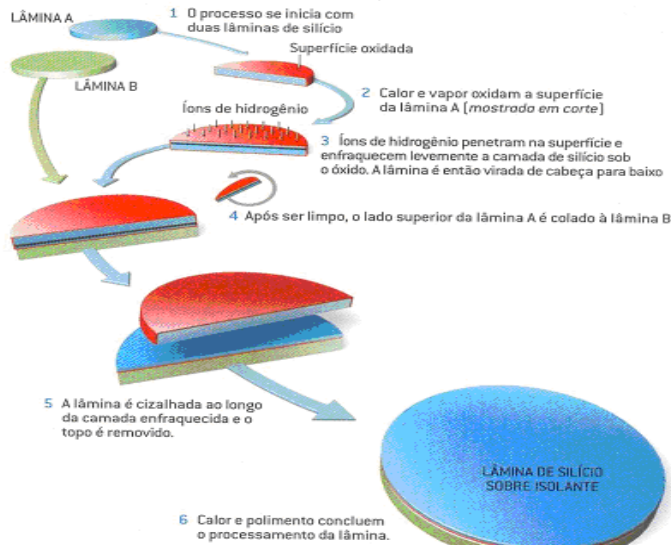


#### REFINAMENTOS NA FABRICAÇÃO DE CHIPS



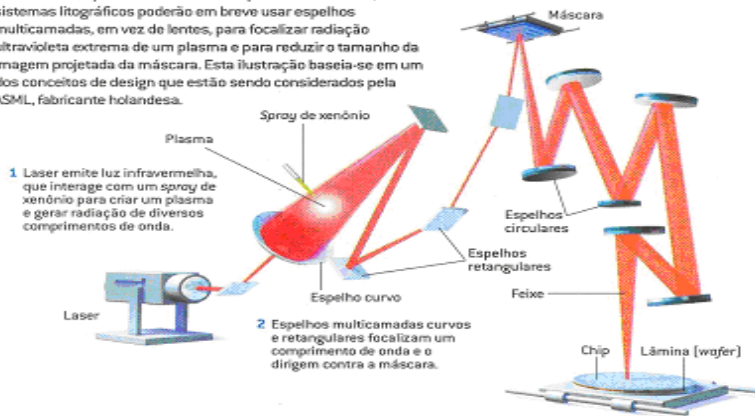
### FATIANDO UM NANOCHIP

A TECNOLOGIA DE SILÍCIO SOBRE ISOLANTE, que ajudou a melhorar consideravelmente o desempenho dos chips, ficou mais barata e mais fácil de ser adotada graças a uma técnica chamada Smart-Cut, desenvolvida pela Soitec, empresa francesa.

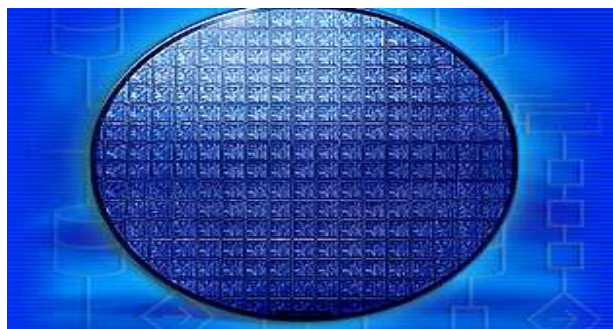


### LITOGRAFIA ULTRAVIOLETA EXTREMA

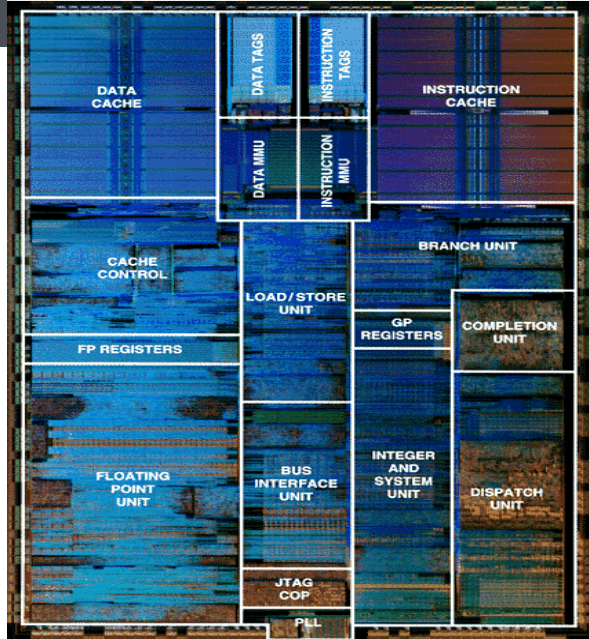
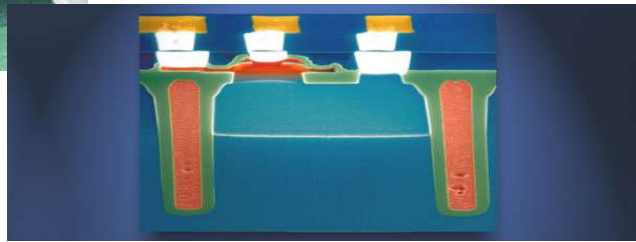
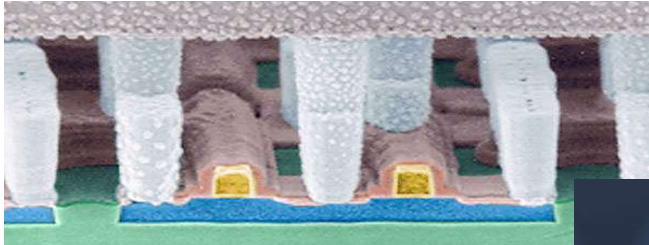
LENTEs que são usadas em sistemas litográficos convencionais absorveriam a luz ultravioleta extrema necessária para formar o padrão de componentes menores do que 50 nm. Por isso, os sistemas litográficos poderão em breve usar espelhos multicamadas, em vez de lentes, para focalizar radiação ultravioleta extrema de um plasma e para reduzir o tamanho da imagem projetada da máscara. Esta ilustração baseia-se em um dos conceitos de design que estão sendo considerados pela ASML, fabricante holandesa.



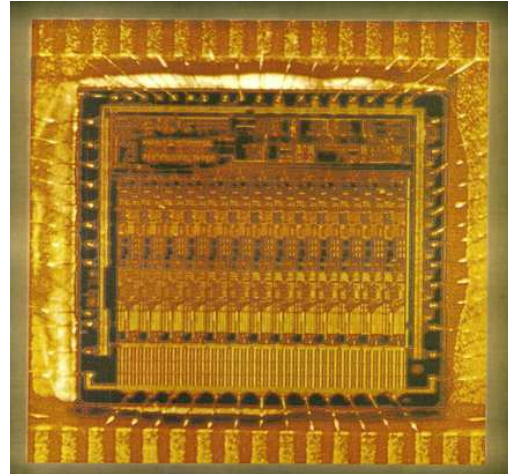
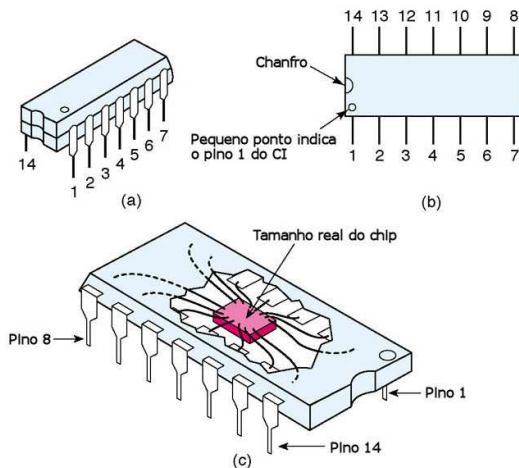
## Wafer



## Chip em Corte



## Encapsulamento



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Lógica Digital

Prof. Edson Pedro Ferlin

## Funções Lógicas

Sistema de alarme de cinto de segurança:

- Sensores para gerar entradas (sensor=1) se estiver ativado.
- Existe um sensor que indica se a marcha (M) está engatada
- É posicionado um sensor sob cada banco frontal (D e E) que será ativado quando alguém ocupa este banco
- Outro tipo de sensor é instalado em cada banco para determinar se o cinto (Cd e Ce) está fechado
- Deve-se acionar a buzina quando a ignição (I) é ligada e a marcha está engatada e contanto que qualquer banco frontal esteja ocupado e o cinto correspondente não esteja fechado.

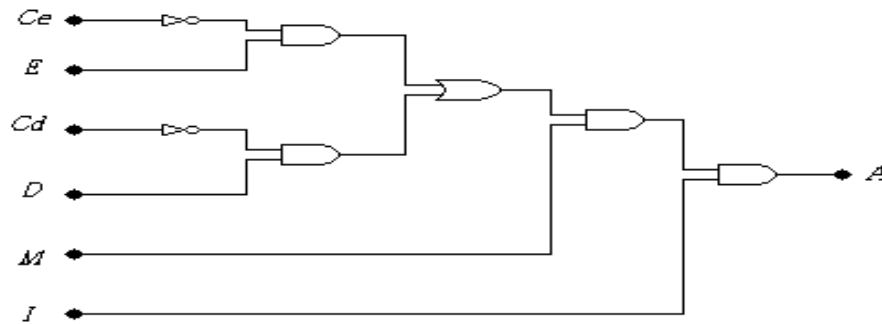
$$A = I . M . \left( (D . \overline{Cd}) + (E . \overline{Ce}) \right)$$

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Lógica Digital

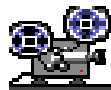
Prof. Edson Pedro Ferlin

## Função Lógica Circuito



## Circuito Eletrônico (como desenhar)

Assista o vídeo sobre Álgebra Booleana  
(link: <https://youtu.be/N0QtxqZid48>).

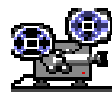


## Tabela Verdade

<i>A</i>	<i>B</i>	<i>C</i>	<i>Y</i>
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

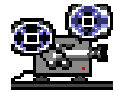
## Equação Lógica

Assista o vídeo sobre Equação Lógica  
(link: <https://youtu.be/Y-r-JLRo6zQ>).



## Álgebra Booleana

Assista o vídeo sobre Álgebra Booleana  
(link: <https://youtu.be/gLMgEG1VuvU>).



Propriedade	Equação
Idempotência ou Equipotência	$x + x = x$ (1)
	$x \cdot x = x$ (1')
Identidade	$x + 1 = 1$ (2)
	$x \cdot 0 = 0$ (2')
	$x + 0 = x$ (3)
	$x \cdot 1 = x$ (3')
Comutatividade	$x + y = y + x$ (4)
	$x \cdot y = y \cdot x$ (4')
Associatividade	$(x + y) + z = x + (y + z)$ (5)
	$(x \cdot y) \cdot z = x \cdot (y \cdot z)$ (5')
Complementação	$x + \bar{x} = 1$ (6)
	$x \cdot \bar{x} = 0$ (6')
Distributividade	$x \cdot (y + z) = (x \cdot y) + (x \cdot z)$ (7)
	$x + (y \cdot z) = (x + y) \cdot (x + z)$ (7')
Teoremas de De Morgan	$\overline{(x + y)} = \bar{x} \cdot \bar{y}$ (8)
	$\overline{(x \cdot y)} = \bar{x} + \bar{y}$ (8')

## Álgebra Booleana

### Propriedades

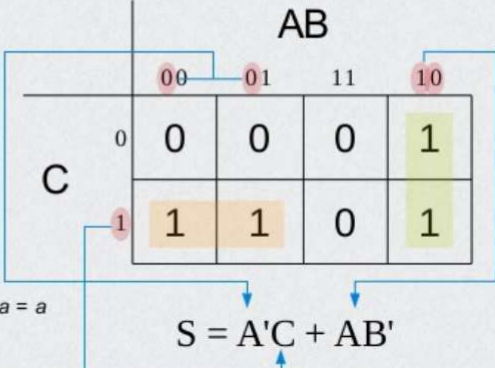
## Simplificação Algébrica

$$\begin{aligned}
 f(x, y) &= x + xy \\
 &= x \cdot 1 + xy && (3) \\
 &= x(1 + y) && (7) \\
 &= x \cdot 1 && (2) \\
 &= x && (3)
 \end{aligned}$$

## Mapa de Karnaugh

A	B	C	S
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Extraia somente as variáveis que não se alteram

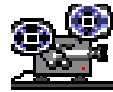


$\Sigma m(1,2,4,6)$   
 $= A'B'C + A'BC + AB'C + AB'C$   
 $= A'C + AC + AB' + AB'$   $\rightarrow a + a = a$   
 $= A'C + AB'$

$S = A'C + AB'$

## Mapa de Karnaugh

Assista o vídeo sobre Mapa de Karnaugh  
(link: <https://youtu.be/y9QrmQ6aWW4>).

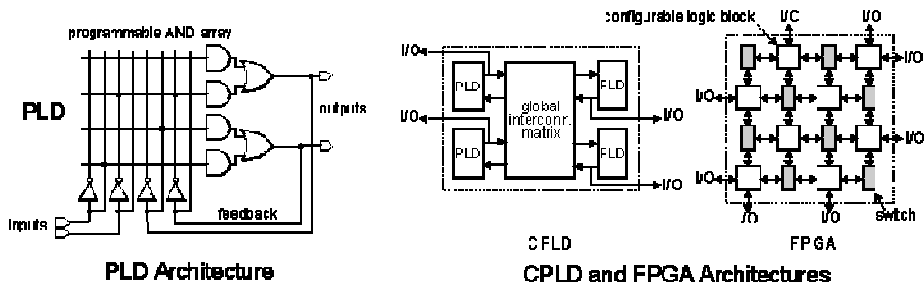


## Método Quine-McCluskey

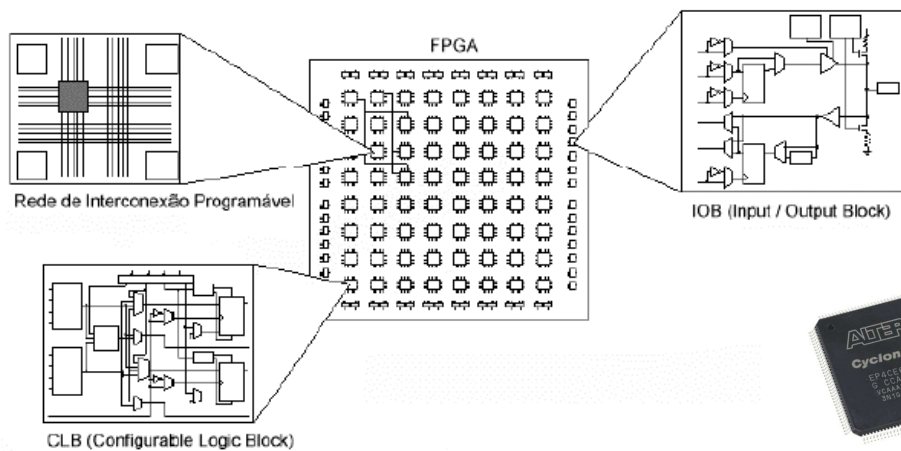
○ **Algoritmo de Quine–McCluskey** (ou **método dos implicantes primos**) é um método utilizado para minimização de funções booleanas desenvolvido por W.V. Quine e Edward J. McCluskey em 1956.

## Dispositivos Reconfiguráveis

PLDs (*Programmable Logic Device*)  
CPLDs (*Complex PLD*)  
FPGAs (*Field-Programmable Gate Array*)

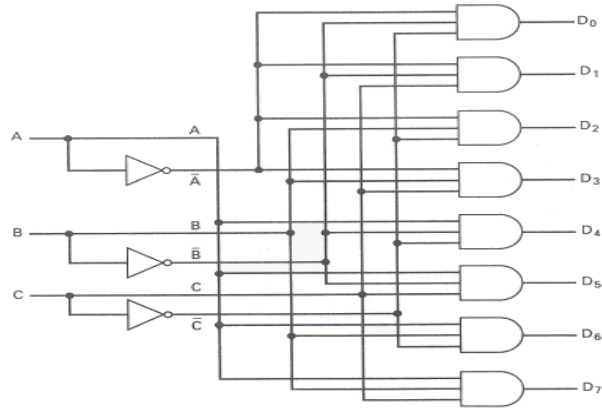


## Arquitetura Interna

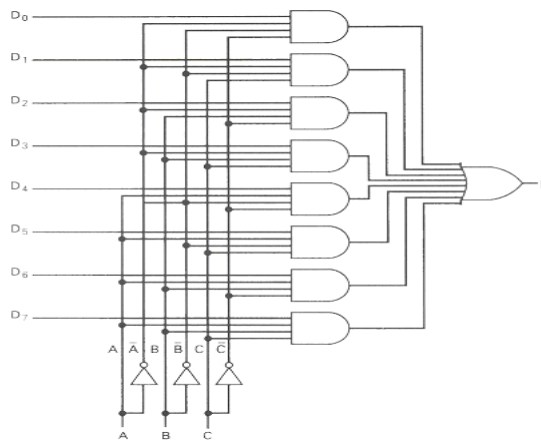




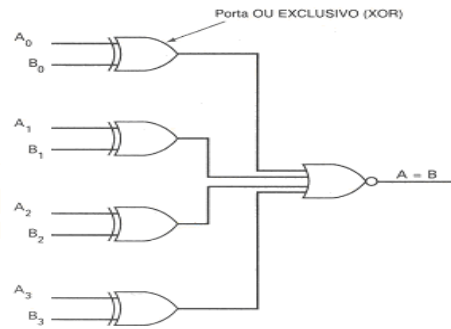
## Decodificador



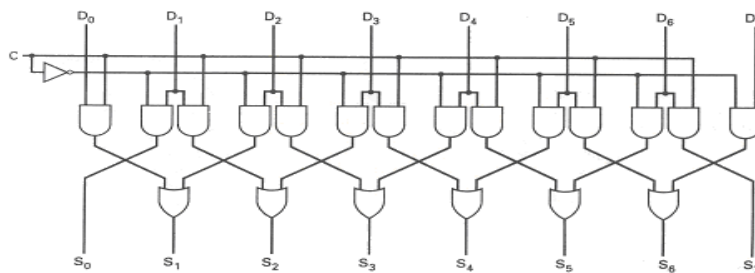
## Multiplexador



## Comparador



## Deslocador

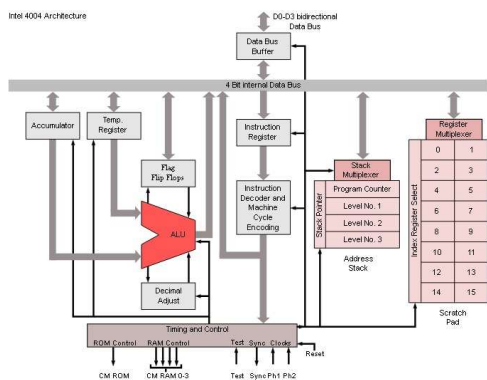


## Aritmética Binária

	Soma	Resto
0 + 0	0	0
0 + 1	1	0
1 + 0	1	0
1 + 1	0	1

- Adição
- Subtração
- Multiplicação
- Divisão

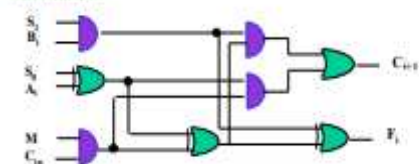
## ULAs - CPUs



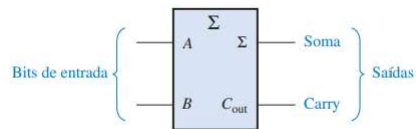
Exemplo de uma ULA Simples de 4 Bits - 12 Entradas, 5 Saídas



cada estágio

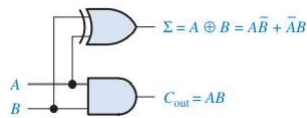


## Meio Somador (Half Adder)

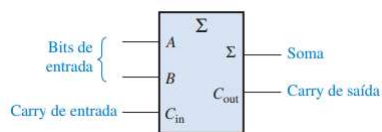


A	B	C <sub>out</sub>	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Σ = soma  
C<sub>out</sub> = carry de saída  
A e B = variáveis de entrada (operandos)

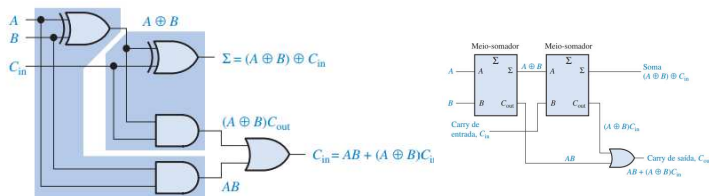


## Somador Completo (Full Adder)



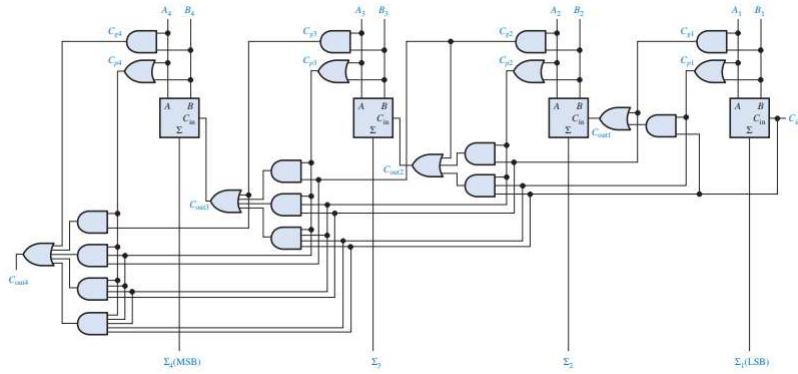
A	B	C <sub>in</sub>	C <sub>out</sub>	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C<sub>in</sub> = carry de entrada, algumas vezes indicado como CI  
C<sub>out</sub> = carry de saída, algumas vezes indicado como CO  
Σ = soma  
A e B = variáveis de entrada (operandos)





## Somador com Carry antecipado



Somador-completo 1:

$$C_{out1} = C_{g1} + C_{p1}C_{in1}$$

Somador-completo 2:

$$C_{in2} = C_{out1}$$

$$C_{out2} = C_{g2} + C_{p2}C_{in2} = C_{g2} + C_{p2}C_{out1} = C_{g2} + C_{p2}(C_{g1} + C_{p1}C_{in1})$$

$$= C_{g2} + C_{p2}C_{g1} + C_{p2}C_{p1}C_{in1}$$

Somador-completo 3:

$$C_{in3} = C_{out2}$$

$$C_{out3} = C_{g3} + C_{p3}C_{in3} = C_{g3} + C_{p3}C_{out2} = C_{g3} + C_{p3}(C_{g2} + C_{p2}C_{g1} + C_{p2}C_{p1}C_{in1})$$

$$= C_{g3} + C_{p3}C_{g2} + C_{p3}C_{p2}C_{g1} + C_{p3}C_{p2}C_{p1}C_{in1}$$

Somador-completo 4:

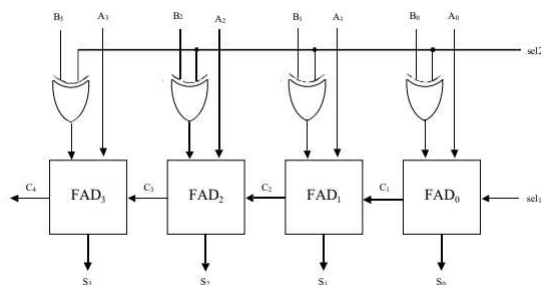
$$C_{in4} = C_{out3}$$

$$C_{out4} = C_{g4} + C_{p4}C_{in4} = C_{g4} + C_{p4}C_{out3}$$

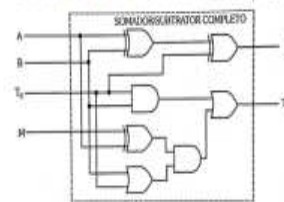
$$= C_{g4} + C_{p4}(C_{g3} + C_{p3}C_{g2} + C_{p3}C_{p2}C_{g1} + C_{p3}C_{p2}C_{p1}C_{in1})$$

$$= C_{g4} + C_{p4}C_{g3} + C_{p4}C_{p3}C_{g2} + C_{p4}C_{p3}C_{p2}C_{g1} + C_{p4}C_{p3}C_{p2}C_{p1}C_{in1}$$

## Somador/Subtrator completo

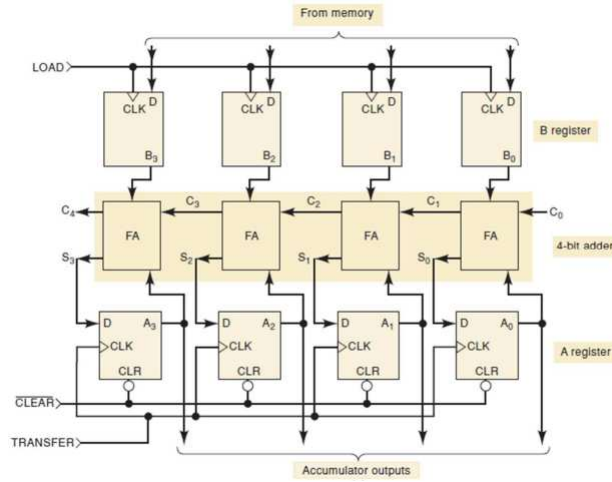


Circuito do Somador/Subtrator Completo:

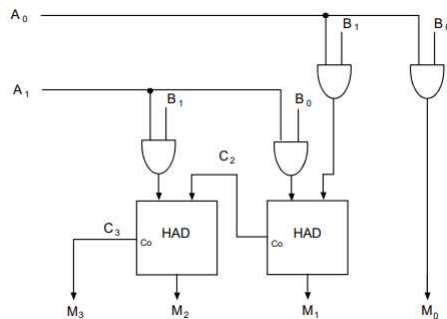


sel2	sel1	operação	descrição
0	0	$S = A + B + 0$	adiciona A e B ( $S = A + B$ )
0	1	$S = A + B + 1$	adiciona A e B incrementado ( $S = A + B + 1$ )
1	0	$S = A + \bar{B} + 0$	subtrai B decrementado de A ( $S = A - B - 1$ )
1	1	$S = A + \bar{B} + 1$	subtrai B de A ( $S = A - B$ )

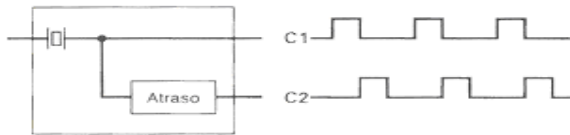
## Somador Completo com Registradores



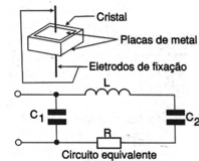
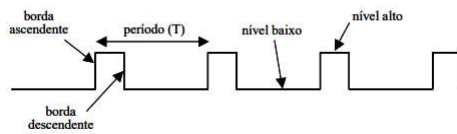
## Multiplicador Binário



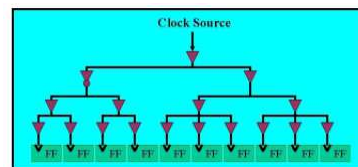
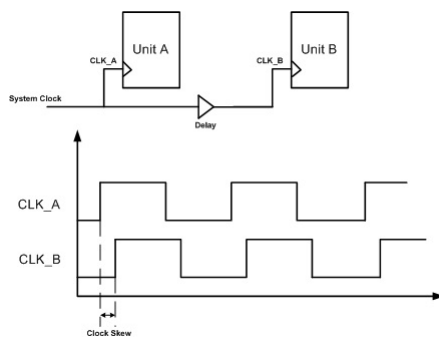
## Clock



$$f = \frac{1}{T}$$



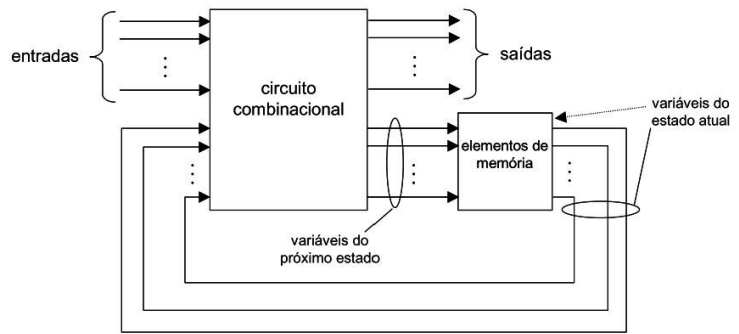
## Distribuição do Clock



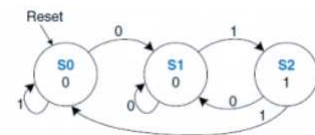
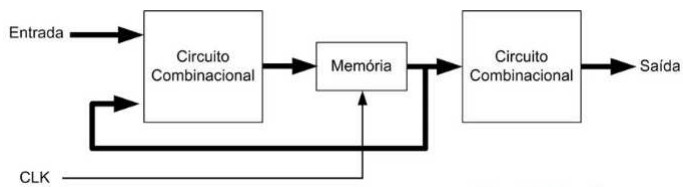
## Circuitos Sequenciais

### Máquina de Estados Finitos (FSM – Finite State Machine)

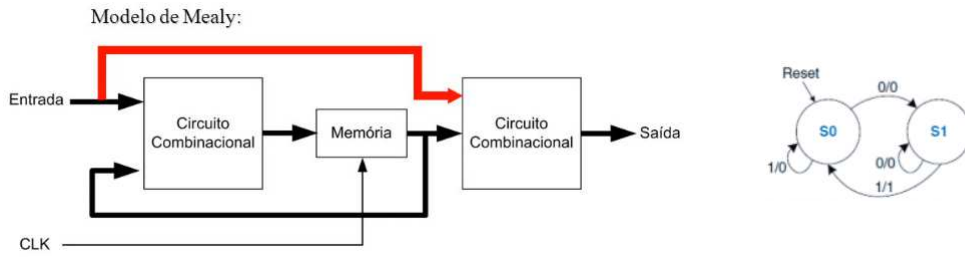
- Mealy → Transições (estados + entradas)
- Moore → Estados



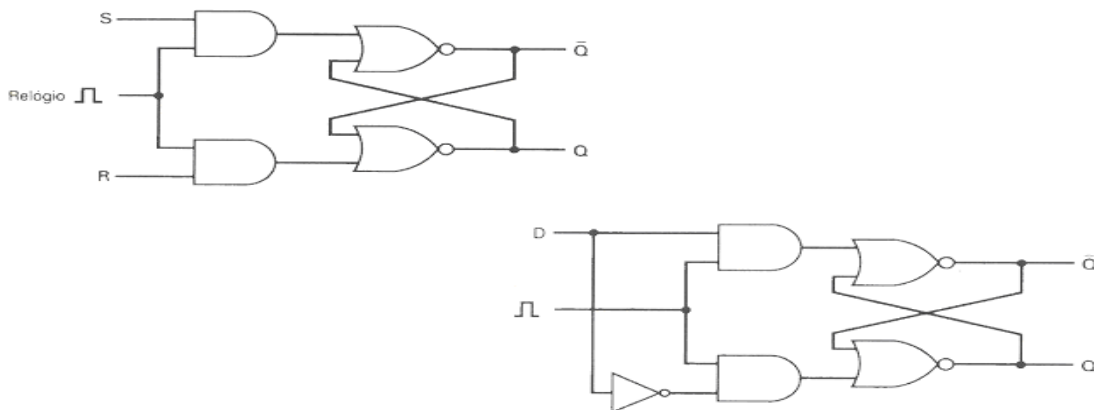
## Máquina de Moore



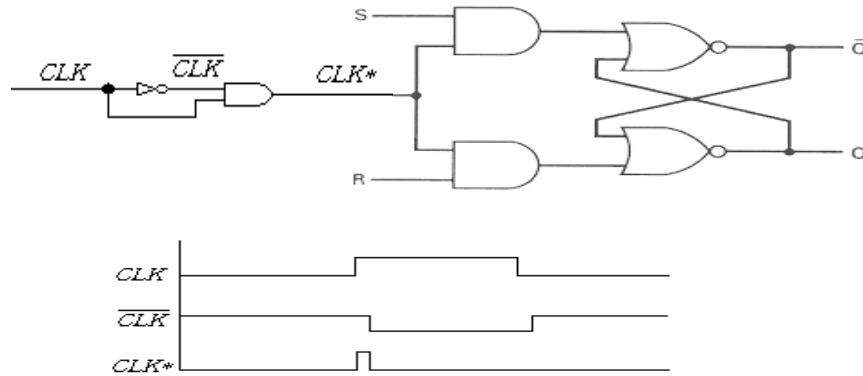
## Máquina de Mealy



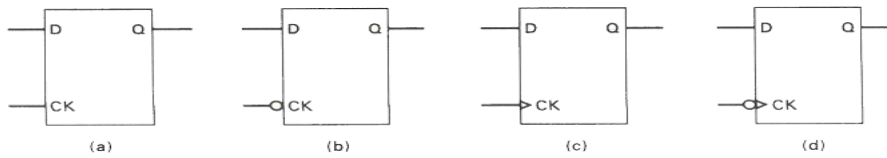
## Latch



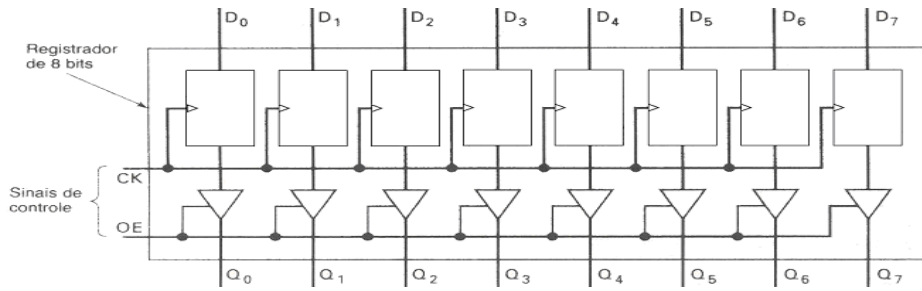
## Flip - Flop



## Flip – Flop x Latch



## Registrador



## Contato



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